#12 Appeal Brief R. Morgan 11/6/98

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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|---|---|
| In re application of: | Adam Stanislaw Wyszynski |
| Serial No.: | 08/579,072 |
| Filed: | December 22, 1995 |
| Art Unit: | 2744 |
| Examiner: | Nay Maung |
| For: | SIGNAL-TO-NOISE OPTIMIZED FULLY MONOLITHIC VIDEO RECEIVER IF CHANNEL |

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Date of deposit September 29, 1998

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By: Maurie Katon

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**Assistant Commissioner for Patents Washington, D.C. 20231**

11-10-98 Received 2341 1700 6-3-99



**ATTENTION: Board of Patent Appeals and Interferences**

## APPELLANT'S BRIEF

This brief is in furtherance of the Notice of Appeal, filed in this case on July 2, 1998.

The fees required under § 1.17(f) and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief is transmitted in triplicate.

1.192 and M.P.E.P. § 1206:



## I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

MicroTune, Inc. of Plano, Texas.

## II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.



## III. STATUS OF CLAIMS

### A. Total Number of Claims in Application

There are 21 claims pending in application.

### B. Current Status of Claims

1. Claims canceled: NONE.

2. Claims withdrawn from consideration but not canceled: NONE.

3. Claims pending: 1-21.

4. Claims allowed: NONE.

5. Claims rejected: 1-21.

**C. Claims On Appeal**

The claims on appeal are claims 1-21.

## IV. STATUS OF AMENDMENTS

Applicant filed an Amendment After Final Rejection on April 28, 1998. The Examiner responded to the Amendment After Final Rejection in an Advisory Action mailed May 18, 1998. In the Advisory Action, the Examiner indicated that Applicants' proposed amendments to claims 1-21, and proposed new claims 22-25, would not be entered.

Accordingly, the claims enclosed herein as Appendix A do not incorporate either the amendments to claims 1-21, or proposed new claims 22-25, as indicated in the paper filed April 28, 1998. However, the claims in Appendix A do incorporate the amendments indicated in the paper filed by Applicant on December 5, 1997.

## V. SUMMARY OF INVENTION

The claimed invention relates to a fully monolithic video signal processing circuit comprising a single substrate (page 4, lines 2-3; page 2. lines 2-4). The circuit has an input for accepting a signal (FIGURE 1)(page 8, lines 11-18). The input signal is converted to an Intermediate Frequency (IF) band in a mixer (11). The IF signals then pass through a low-

pass filter (12) before passing through a Variable Gain Amplifier (VGA) (13). Following the VGA (13) the signals pass through a band-pass filter (14) and a Fixed Gain Amplifier (FGA)(15).

The VGA (13) detects the amplitude of accepted signals and amplifies the accepted signals to a specific level. Preferably, the signal is amplified by the VGA (13) to the maximum possible signal that the band-pass filter (14) can receive (page 8, line 15-21). If additional gain is needed at the output of the circuit, it is provided by the FGA (15)(page 8, line 21). As a result, any noise introduced into by the band-pass filter (14) is only amplified by the FGA (15) (page 8, lines 23-25).

In order to achieve an optimum signal to noise ratio, the VGA (13) ensures that the band-pass filter (14) always receives the maximum possible input signal (page 4, lines 7-8). Since the signal input level to the band-pass filter (14) is kept constant, the band-pass filter's linear range is optimized which reduces distortion and saves on dissipated power (page 4, lines 14-19).

## VI. ISSUES

Whether claims 1-12 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,361,395 to Yamamoto in view of U.S. Patent No. 5,491,507 to Umezawa et al.

Whether claims 13-22 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,361,395 to Yamamoto in view of U.S. Patent No. 5,555,550 to Kaschke.

## VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below:

| Group | Claim(s) |
|---|---|
| I. | 1, 2, 3, 4 and 5 |
| II. | 6 |
| III. | 7, 8, 9, 10 and 11 |
| IV. | 12 |
| V. | 13, 15, 16 and 17 |
| VI. | 14 |
| VII. | 18, 20 and 21 |
| VIII. | 19 |

In Section VIII below, Applicant has included arguments supporting the separate patentability of each claim group as required by M.P.E.P. § 1206.

## VIII. ARGUMENTS

Claims 1-12 have been rejected as unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,361,395 to Yamamoto (*Yamamoto)* in view of U.S. Patent No. 5,491,507 to Umezawa et al. (*Umezawa*).

### CLAIM 1

The Examiner has rejected claim 1 under 35 U.S.C. § 103(a) as unpatentable over *Yamamoto* in view of *Umezawa*. Claim 1 is directed to a monolithic video signal processing circuit which requires "means . . . for processing said amplified [video] signals". *Yamamoto* discloses an AGC circuit for receiving audio signals on a mobile telephone. *Umezawa* discloses the mechanical construction of a video telephone. However, neither reference teaches or suggests a means for processing video signals as required by claim 1. Accordingly, Applicant traverses the rejection of claim 1 as obvious in view of *Yamamoto* and *Umezawa*.

The Examiner suggests that *Umezawa* teaches "telephone equipment for receiving and transmitting a voice signal and a video signal." (Final Office Action, page 3). The *Umezawa* reference discloses five physical embodiments of a mobile video telephone (first embodiment, column 5, line 26; second embodiment, column 12, line 13; third embodiment, column 14, line 62; fourth embodiment, column 16, line 46; and fifth embodiment, column 18, line 37). Applicant submits that *Umezawa* is effectively a design patent for a mobile

phone because there is no discussion of actual voice or video signal processing. The extent of the disclosure that relates to signal processing is the identification of a "main circuit board 17 which includes a processor and a memory" (column 5, lines 56-57). Main circuit board 17 is shown as a nondescript box in the drawings for the first embodiment (Figures 3 and 4) and it is not shown at all in the drawings for the other four embodiments.

The *Umezawa* disclosure contains no discussion of the components of a circuit or apparatus for signal processing. However, the *Umezawa* claims do include "signal processing means for permitting at least either of a vocal communication or a visual communication." 35 U.S.C. § 112, paragraph six, states that a "means for" claim element is "construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." In view of § 112, the "signal processing means" of *Umezawa* only covers the non-enabling block labeled 17 in Figures 3 and 4. This disclosure is clearly insufficient to teach any form of video or visual communications signal processing.

M.P.E.P. § 2143.01 requires that there be some suggestion or motivation to combine prior art references in order to establish obviousness. There is no motivation to combine the non-enabling *Umezawa* disclosure with any other reference in order to teach signal processing. Applicant submits that undue experimentation would be required by one skilled in the art in order to make or use the *Umezawa* device. The Examiner admits that *Yamamoto* does not teach "accepting a signal is a video signal" (sic) (Final Office Action, page 3). Therefore, at best, if one skilled in the art looked to *Yamamoto* or *Umezawa*, he or she would only find a "signal processing means for permitting . . . a vocal communication." Accordingly, even if the Examiner could show motivation to make this combination, it would not yield the claimed video signal processing circuit of claim 1.

M.P.E.P. § 2143.03 requires that all claim limitations must be taught or suggested by the prior art for a *prima facie* case of obviousness. The *Yamamoto* and *Umezawa* references not only fail to teach or suggest a monolithic or integrated circuit, as discussed above, but they also fail to teach or suggest any form of video signal processing circuit or apparatus, such as the "means . . . for processing said amplified signals to reduce all but the intermediate frequencies (IF) present in said video signals" as required in claim 1.

In view of the preceding remarks, Applicant submits that the combination of

*Yamamoto* and *Umezawa* cannot satisfy the requirements of a *prima facie* case of obviousness under M.P.E.P. § 2143. Therefore, claim 1 is allowable over the cited references under 35 U.S.C. § 103(a) and should be passed to issue.

**CLAIMS 2, 3, 4 AND 5**

For the purpose of this appeal brief, claims 2-5 are grouped with claim 1. However, since claims 2-5 depend directly or indirectly from claim 1, they remain patentable over the combination of *Yamamoto* and *Umezawa* by comprising the non-obvious limitations of claim 1 in addition to further comprising the limitations in each of the dependent claim 2-5.

**CLAIM 6**

Claim 6 depends from claim 1 and further requires that the "specific level" is a "maximum level acceptable as an input to said processing means to avoid distortion of said video signal." The Examiner has cited column 4, lines 1-20, of *Yamamoto* as teaching this limitation. However, the cited portion of *Yamamoto* merely discloses that the cited amplifier is a "level control means" (column 4, lines 13-14). There is no teaching or suggestion in *Yamamoto* that amplifier **16** is used to amplify the signal to a "maximum level acceptable" to filter **17** to "avoid distortion." Instead, amplifier **16** is part of a typical AGC circuit and is controlled by level detector **1** and error amplifier **4** to maintain a level signal at the **output** of filter 17, not at the **input** of filter 17 as required in claim 6.

Accordingly, *Yamamoto* and *Umezawa* do not teach each and every element of claim 6 as required for obviousness under 35 U.S.C. § 103(a). Furthermore, claim 6 requires the elements of claim 1 which are not taught or suggested by the cited combination as discussed above. Therefore, claim 6 is allowable over the combination of the *Yamamoto* and *Umezawa* references and should be passed to issue.

Claim 6 comprises limitations that are patentably distinct from claims 1-5 and from *Yamamoto,* and *Umezawa*. Therefore, claim 6 stands alone for the purpose of this appeal and is independently and separately patentable.

**CLAIM 7**

The Examiner has rejected claim 7 under 35 U.S.C. § 103(a) as unpatentable over *Yamamoto* in view of *Umezawa*. Claim 7 is directed to a method of processing a video signal which requires the step of "presenting said video signal to the input of a monolithic circuit." *Yamamoto* discloses an AGC circuit for receiving audio signals on a mobile telephone. *Umezawa* discloses the mechanical construction of a video telephone. However, neither reference teaches or suggests processing a video signal on a monolithic circuit as required in claim 7. Accordingly, Applicant traverses the rejection of claim 7 in view of the *Yamamoto* and *Umezawa* combination.

In the rejection of claims 13-21, the Examiner cited the *Kaschke* reference in response to Applicant's argument that the *Yamamoto* and *Umezawa* failed to teach a monolithic circuit. The Examiner also cited a textbook definition of "monolithic" in which monolithic integrated circuit is defined to mean a circuit built on a single crystal of silicon. Applicant submits that this definition supports the argument that the printed circuit substrate of *Kaschke* is not a monolithic circuit as required by the claims and as defined in the cited dictionary definitions.

As discussed above with respect to claim 1, the *Umezawa* disclosure contains no discussion of the components of a circuit or apparatus for signal processing. Instead, the "signal processing means" of *Umezawa* only covers the non-enabling block labeled "17" in Figures 3 and 4. This disclosure is clearly insufficient to teach any form of video or visual communications signal processing.

M.P.E.P. § 2143.01 requires that there be some suggestion or motivation to combine prior art references in order to establish obviousness. There is no motivation to combine the non-enabling *Umezawa* disclosure with any other reference in order to teach signal processing. Applicant submits that undue experimentation would be required by one skilled in the art in order to make or use the *Umezawa* device. The Examiner admits that *Yamamoto* does not teach "accepting a signal is a video signal" (sic). (Final Office Action, page 3). Therefore, at best, if one skilled in the art looked to *Yamamoto* or *Umezawa*, he or she would only find a "signal processing means for permitting . . . a vocal communication." and looking to one could find (at best) a visual processor for use within the mobile telephone spectrum. Even if the Examiner could show motivation to make this combination, it would not yield the claimed video signal processing method of claim 7.

The *Yamamoto* invention is directed to controlling an automatic gain control (AGC) circuit in a mobile telephone receiver. The *Yamamoto* disclosure contains twelve figures, and their related descriptions, which show various circuits that employ the AGC circuit. However, despite the numerous combinations of elements that are shown, *Yamamoto* fails to include any discussion of design considerations for any of the embodiments. Most pertinent to the present application is the lack of any discussion related to an integrated or monolithic embodiment of the *Yamamoto* receiver circuit. Furthermore, the disclosure lacks any reference to integrated or monolithic circuit design considerations, such as detrimental noise characteristics or electronic coupling between elements on an integrated substrate. Accordingly, it is apparent that the *Yamamoto* reference does not contemplate constructing the claimed elements on a single integrated substrate.

M.P.E.P. § 2143.03 requires that all claim limitations must be taught or suggested by the prior art for a *prima facie* case of obviousness. The *Yamamoto* and *Umezawa* references not only fail to teach or suggest a monolithic or integrated circuit, as discussed above, but they also fail to teach or suggest any method for video signal processing as required in claim 7.

In view of the preceding remarks, Applicant submits that the combination of *Yamamoto* and *Umezawa* cannot satisfy the requirements of a *prima facie* case of obviousness under M.P.E.P. § 2143. Therefore, claim 7 is allowable over the cited references under 35 U.S.C. § 103(a) and should be passed to issue.

Claims 7-11 comprises limitations that are distinct from claims 1-6 and from *Yamamoto, and Umezawa.* Therefore, although claims 7-11 stand as a group for the purpose of this appeal and each claim is independently and separately patentable.

**CLAIMS 8, 9, 10 AND 11**

For the purpose of this appeal brief, claims 8-11 are grouped with claim 7. However, since claims 8-11 depend directly or indirectly from claim 1, they remain patentable over the combination of *Yamamoto* and *Umezawa* by comprising the non-obvious limitations of claim 7 in addition to further limitations in each dependent claim 8-11.

**CLAIM 12**

Claim 12 depends from claim 7 and further requires that the "specific level for said amplification is the maximum level acceptable as an input to said further processing means to avoid distortion of said video signal." The Examiner has cited column 4, lines 1-20, of *Yamamoto* as teaching this limitation. However, the cited portion of *Yamamoto* merely discloses that the cited amplifier is a "level control means" (column 4, lines 13-14). There is no teaching or suggestion in *Yamamoto* that amplifier **16** is used to amplify the signal to a "maximum level acceptable" to filter **17** to "avoid distortion." Instead, amplifier **16** is part of a typical AGC circuit and is controlled by level detector **1** and error amplifier **4** to maintain a level signal at the **output** of filter 17, not at the **input** of filter 17 as required by the limitation of "**accepting** said specific level amplified video signals and further processing said amplified signals" in claim 7.

Accordingly, *Yamamoto* and *Umezawa* do not teach each and every element of claim 12 as required for obviousness under 35 U.S.C. § 103(a). Furthermore, claim 12 requires the elements of claim 7 which are not taught or suggested by the cited combination as discussed above. Therefore, claim 12 is allowable over the combination of the *Yamamoto* and *Umezawa* references and should be passed to issue.

Claim 12 comprises limitations that are distinct from claims 1-11 and from *Yamamoto,* and *Umezawa*. Therefore, claim 12 stands alone for the purpose of this appeal and is independently and separately patentable.

Claims 13-22 have been rejected as unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,361,395 to Yamamoto (*Yamamoto*) in view of U.S. Patent No. 5,555,550 to Kaschke (*Kaschke*).

**CLAIM 13**

Claim 13 stands rejected as unpatentable over *Yamamoto* in view of *Kaschke*. The Examiner admits that *Yamamoto* does not teach constructing mixers, filters and amplifiers on an integrated substrate. (Final Office Action, page 4). However, the *Kaschke* reference is

used to show that "putting the electrical components on a single integrated substrate circuit is very well-known in the art." (Final Office Action, page 4.). Applicant traverses the obviousness rejection of claim 13 and submits that the *Yamamoto* and *Kaschke* references, either individually or in combination, do not teach or suggest every element of rejected claim 13.

*Kaschke* **does not** teach putting electrical components, such as the claimed mixers, filters and amplifiers, on the same monolithic circuit or integrated substrate. Instead, the only type of electrical component discussed in the *Kaschke* disclosure is an LED that is used for a cellular telephone display. There is no discussion of RF or IF signal processing components, such as those elements required by claim 13, in the *Kaschke* reference. LEDs for a telephone display are not equivalent to the claimed mixers, filters, and amplifiers.

Moreover, the *Kaschke* LEDs are **surface mount** components that are mounted on a **printed circuit** substrate (column 3, lines 30-32). *Kaschke* does not teach components that are **constructed on an integrated circuit substrate** as required in claim 13. *Kaschke's* teachings that LEDs can be mounted on printed circuits cannot be extended to suggest constructing monolithic RF and IF components, such as mixers, filters and amplifiers, because the *Kaschke* disclosure does not address the problems discussed in the Application, such as the lack of inductors in integrated circuits and the signal-to-noise considerations for integrated RF circuits. Furthermore, neither *Yamamoto* nor *Kaschke* suggest any way to overcome these problems. Therefore, the proposed combination does not provide any motivation to combine the references under M.P.E.P. § 2143.01, or teach or suggest the required claim limitations under M.P.E.P. § 2143.03.

In view of the preceding remarks, Applicant submits that the combination of *Yamamoto* and *Kaschke* cannot satisfy the requirements of a *prima facie* case of obviousness under M.P.E.P. § 2143. Therefore, claim 13 is allowable over the cited references under 35 U.S.C. § 103(a) and should be passed to issue.

Claims 13, 15-17 comprises limitations that are distinct from claims 1-12 and 14 and from *Yamamoto, and Kaschke.* Therefore, although claims 13, 15-17 stand as a group for the purpose of this appeal and each claim is independently and separately patentable.

**CLAIM 14**

Claim 14 depends from claim 13 and additionally requires a low-pass filter. The Examiner admits that *Yamamoto* does not teach a low-pass filter. (Final Office Action, page 5). In order to provide the low-pass filter limitation, the Examiner suggests that low-pass and band-pass filters are interchangeable solely based upon cost. (Final Office Action, page 5). Applicant traverses the suggested modification in which filters are exchanged without any showing of technical feasibility. Applicant submits that there is no motivation to make such a modification to the *Yamamoto* system and that there is no technical basis for such a change. Therefore, simply replacing a band-pass filter with a low-pass filter has no reasonable expectation of success under M.P.E.P. § 2143.02.

In response to Applicant's previous objections to the assertion that band-pass and low-pass filters are inter-changeable, the Examiner provided dictionary definitions of "low-pass filter" and "band-pass filter" and quoted a **portion** of each definition. However, a comparison of the **full** definitions clearly shows that low-pass and band-pass filters **are not equivalent** according to the cited technical dictionary. For example,

> **band-pass filter** . . . . A wave filter that has a single transmission band, *neither of the cut-off frequencies being zero* or infinite.

THE NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS 90 (5th ed. 1993)(emphasis added);

> **filter, low-pass**. A filter having a single transmission band *extending from zero to some cutoff frequency*, not infinite.

*Id.* at 500 (emphasis added).

Applicant submits that a **partial** citation of dictionary definitions in the final Office Action was not a clear and complete response to Applicant's arguments as required under M.P.E.P. § 707.07. Furthermore, such a **partial** quoting of the filter definitions fails to show that exchanging low-pass and band-pass filters is obvious. The Examiner has only cited the portion of the definitions which support the proposition that low-pass filters are equivalent to band-pass filters, while ignoring the contradictory portions of the definitions. Additionally, the Examiner has not provided a prior art reference or affidavit that teaches exchanging low-pass and band-pass filters based merely upon **cost** without regard to any **technical**

considerations. Accordingly, Applicant respectfully requests that the Examiner withdraw the final rejection of claim 14 and reconsider the application in view of the remarks herein.

Claim 14 comprises limitations that are distinct from claims 1-13 and 15-17 and from *Yamamoto,* and *Kaschke*. Therefore, claim 14 stands alone for the purpose of this appeal and is independently and separately patentable.

**CLAIMS 15, 16 AND 17**

For the purposes of this appeal brief, claims 15-17 are grouped with claim 13. However, since claims 15-17 depend directly from claim 15, they remain patentable over the combination of *Yamamoto* and *Kaschke* by comprising the non-obvious limitations of claim 13 in addition to further limitations in each dependent claim 15-17.

**CLAIM 18**

Claim 18 stands rejected as unpatentable over *Yamamoto* in view of *Kaschke*. The Examiner admits that *Yamamoto* does not teach constructing mixers, filters and amplifiers on an integrated substrate. (Final Office Action, page 4). However, the *Kaschke* reference is used to show that "putting the electrical components on a single integrated substrate circuit is very well-known in the art." (Final Office Action, page 4.). Applicant traverses the obviousness rejection of claim 18 and submits that the *Yamamoto* and *Kaschke* references, either individually or in combination, do not teach or suggest every element of rejected claim 18.

*Kaschke* **does not** teach putting electrical components, such as mixers, filters and amplifiers, on the same monolithic circuit or integrated substrate. Instead, the only type of electrical component discussed in the *Kaschke* disclosure is an LED that is used for a cellular telephone display. There is no discussion of RF or IF signal processing components, such as those elements required by claim 18, in the *Kaschke* reference. LEDs for a display are not equivalent to the mixers, filters, and amplifiers.

Moreover, the *Kaschke* LEDs are **surface mount** components that are mounted on a **printed circuit** substrate (column 3, lines 30-32). *Kaschke* does not teach components that are **constructed on an integrated circuit substrate** as required in claim 18. *Kaschke's*

teachings that LEDs can be mounted on printed circuits cannot be extended to suggest constructing monolithic RF and IF components, such as mixers, filters and amplifiers, because the *Kaschke* disclosure does not address the problems discussed in the Application, such as the lack of inductors in integrated circuits and the signal-to-noise considerations for integrated RF circuits. Furthermore, neither *Yamamoto* nor *Kaschke* suggest any way to overcome these problems. Therefore, the proposed combination does not provide any motivation to combine the references under M.P.E.P. § 2143.01, or teach or suggest the required claim limitations under M.P.E.P. § 2143.03.

In view of the preceding remarks, Applicant submits that the combination of *Yamamoto* and *Kaschke* cannot satisfy the requirements of a *prima facie* case of obviousness under M.P.E.P. § 2143. Therefore, claim 18 is allowable over the cited references under 35 U.S.C. § 103(a) and should be passed to issue.

Claims 18, 20 and 21 comprises limitations that are distinct from claims 1-17 and 19 and from *Yamamoto, and Kaschke.* Therefore, although claims 18, 20 and 21 stand as group for the purpose of this appeal and each claim is independently and separately patentable.

**CLAIM 19**

Claim 19 depends from claim 18 and additionally requires a low-pass filter. The Examiner admits that *Yamamoto* does not teach a low-pass filter. (Final Office Action, page 5). In order to provide the low-pass filter limitation, the Examiner suggests that low-pass and band-pass filters are interchangeable solely based upon cost. (Final Office Action, page 5). Applicant traverses any modification in which filters are exchanged without any showing of technical feasibility. Applicant submits that there is no motivation to make such a modification to the *Yamamoto* system and that there is no technical basis for such a change. Therefore, simply replacing a band-pass filter with a low-pass filter has no reasonable expectation of success under M.P.E.P. § 2143.02.

In response to Applicant's previous objections to the assertion that band-pass and low-pass filters are inter-changeable, the Examiner provided dictionary definitions of "low-pass filter" and "band-pass filter" and quoted a **portion** of each definition. However, a comparison of the **full** definitions clearly shows that low-pass and band-pass filters **are not**

**equivalent** according to the cited technical dictionary. For example,

> **band-pass filter** . . . . A wave filter that has a single transmission band, *neither of the cut-off frequencies being zero* or infinite.

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> **filter, low-pass**. A filter having a single transmission band *extending from zero to some cutoff frequency*, not infinite.

*Id.* at 500 (emphasis added).

Applicant submits that a **partial** citation of dictionary definitions in the final Office Action was not a clear and complete response to Applicant's arguments as required under M.P.E.P. § 707.07. Furthermore, such a **partial** quoting of the filter definitions fails to show that exchanging low-pass and band-pass filters is obvious. The Examiner has only cited the portion of the definitions which support the proposition that low-pass filters are equivalent to band-pass filters, while ignoring the contradictory portions of the definitions. Additionally, the Examiner has not provided a prior art reference or affidavit that teaches exchanging low-pass and band-pass filters based merely upon **cost** without regard to any **technical** considerations. Accordingly, Applicant respectfully requests that the Examiner withdraw the final rejection of claim 14 and reconsider the application in view of the remarks herein.

Claim 19 comprises limitations that are distinct from claims 1-18, 20 and 21 and from *Yamamoto,* and *Kaschke*. Therefore, claim 19 stands alone for the purpose of this appeal and is independently and separately patentable.

## CLAIM 20 AND 21

For the purposes of this appeal brief, claims 20 and 21 are grouped with claim 18. However, since claims 20 and 21 depend indirectly from claim 18, they remain patentable over the combination of *Yamamoto* and *Kaschke* by comprising the non-obvious limitations of claim 18 in addition to further limitations in each dependent claim 20 and 21.

## IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal are attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Applicant on December 5, 1997, and do not include the amendments filed on April 28, 1998.

Respectfully submitted,

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Date: September 29, 1998

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A

**Claims Involved in the Appeal of Application Serial No. 08/579,072**

1. A monolithic video signal processing circuit comprising within a single substrate:

means for accepting a video signal;

means for detecting the amplitude of accepted signals and for amplifying said accepted signals to a specific level; and

means for accepting said specific level amplified video signals and for processing said amplified signals to reduce all but the intermediate frequencies (IF) present in said video signals while amplifying said IF frequencies to a certain fixed value for presentation to an output of said circuit.

2. The invention set forth in claim 1 further comprising:

means connected between said output of said circuit and said processing means for accepting said presented signals and for amplifying said accepted signals a fixed amount.

3. The invention set forth in claim 2 wherein said amplification by said last-mentioned means is low with respect to said amplification by said detecting and amplifying means.

4. The invention set forth in claim 1 wherein said detecting and amplification means is a variable gain amplifier (VGA).

5. The invention set forth in claim 1 wherein said accepting means includes: means for removing therefrom certain unwanted frequencies.

6. The invention set forth in claim 1 wherein said specific level for said amplification is the maximum level acceptable as an input to said processing means to avoid distortion of said video signal.

7. The method of processing a video signal comprising the steps of:

presenting said video signal to the input of a monolithic circuit;

detecting the amplitude of presented signals and amplifying said presented signals to a specific level;

accepting said specific level amplified video signals and further processing said amplified signals to reduce all but the intermediate frequencies (IF) present in said video signals while amplifying said IF frequencies to a certain fixed value for presentation to an output of said monolithic circuit.

8. The method set forth in claim 1 further comprising the step of:

accepting said presented signals before presentation to said output of said monolithic circuit and amplifying said accepted signals a fixed amount, and

presenting said fixed amount amplified signal to said output of said monolithic circuit.

9. The method set forth in claim 8 wherein said last-mentioned amplification is low with respect to the amplification of the detection and amplification step.

10. The method set forth in claim 7 wherein the amplification of the amplification and detection step is accomplished by a variable gain amplifier (VGA).

11. The method set forth in claim 7 further including the step of:

ahead of said detection and amplification step removing from the presented video signal certain unwanted frequencies.

12. The method set forth in claim 7 wherein said specific level for said amplification is the maximum level acceptable as an input to said further processing step to avoid distortion of said video signal.

13. A circuit for processing radio frequency (RF) signals comprising:

an input to said circuit for receiving an RF signal;

a mixer having an input connected to said RF signal input;

a first filter having an input connected to an output of said mixer;

a first amplifier having an input connected to an output of said first filter;

a second filter having an input connected to an output of said first amplifier; and

a second amplifier having an input connected to an output of said second filter, and an output connected to an output of said circuit;

wherein said mixer, said first and second filters and said first and second amplifiers are constructed on a single integrated substrate.

14. The system as claimed in claim 13, wherein said first filter is a low-pass filter.

15. The system as claimed in claim 13, wherein said first amplifier means is a variable gain amplifier (VGA).

16. The system as claimed in claim 13, wherein said second filter means is an intermediate frequency, band-pass filter.

17. The system as claimed in claim 13, wherein said second amplifier means is [an] a fixed gain amplifier (FGA).

18. A method of processing radio frequency (RF) signals, the method comprising the steps of:

receiving an input RF signal;

mixing said input RF signal with an operating frequency signal to generate a first signal;

filtering said first signal to generate a second signal;

amplifying to a fixed level said second signal to generate a third signal;

filtering said third signal to generate a fourth signal; and

amplifying said fourth signal a fixed amount to generate a fifth signal;

wherein said mixing, filtering and amplifying steps are performed on a single integrated substrate.

19. A method for processing RF signals as recited in claim 18, wherein said step of filtering said first signal to generate said second signal includes processing said first signal through a low-pass filter; and

wherein said step of amplifying said second signal to generate a third signal includes amplifying said second signal by a variable gain amplifier (VGA), the limit of said VGA being the maximum level acceptable by said third signal filtering step without distortion.

20. A method for processing RF signals as recited in claim 19, wherein the step of filtering said third signal to generate a fourth signal includes processing said third signal through an intermediate-frequency, band-pass filter.

21. A method of processing RF signals as recited in claim 20, wherein said step of amplifying said fourth signal to generate a fifth signal includes amplifying said fourth signal by a fixed gain amplifier (FGA).